

REMARKS

I. INTRODUCTION

Claims 1-12 were presented originally. The examiner mailed an Office Action on November 30, 2005 requiring Election/Restriction from among three inventions. In a Response to Restriction Requirement dated March 10, 2006, Applicant elected claims 3-6 without traverse and withdrew claims 1-2 and 7-12 from consideration.

In a Revised Response to Restriction Requirement dated April 20, 2006, applicant added new claims 13-46 and 48-49. Applicant did not include a claim numbered 47 in the April 20, 2006 Response, which apparently was a clerical error on Applicant's part.

In the Office Action mailed July 27, 2006, the Examiner rejected claims 3-6 and 13-49.

In the above current Amendment submitted herewith, Applicant has canceled claims 1-2 and 7-12, has amended claims 3, 5, 6, 13-31, 34-40 and 48-49, and has added new claims 50-66.

Therefore, claims 3-6 and 13-46 and 48-66 are pending in the application.

II. CLAIMS OVERVIEW

In response to the Restriction Requirement, Applicant elected:

Group II: Claims 3-6, drawn to a method of determining aggressor-induced delay change with voltage dependent current model and interconnect model, classified in class 703, subclass 19.

Applicant respectfully submits that each of the claims currently pending fall within the elected class and subclass in that each claim sets forth a "current model".

Claims 3 and 40 are independent claims that recite a of determining aggressor-induced delay change with voltage dependent current model and interconnect model. Independent claims 57 and 61 set forth corresponding computer programs encoded in computer readable media for implementing the methods of 3 and 40 respectively.

Independent claims 13 and 19 set forth a "current model" encoded in computer readable media. Independent claims 21 and 31 set forth a computer program encoded in computer

readable media for determining the values in the table used by a "current model".

Independent claim 34 sets for a computer program encoded in computer readable media for using the "current model" to propagating a transition in the presence of an aggressor-induced current waveform.

III. OFFICE ACTION DATED JULY 27, 2006

A. Cancellation of claims 1-2 and 7-12

In paragraph (1) of the Office Action, the Examiner noted that non-elected claims 1-2 and 7-12 had not been canceled. In the above current Amendment, Applicant has canceled claims 1-2 and 7-12. However, Applicant expressly reserve the right to pursue these claims in one or more divisional patent applications.

B. Claim Objections under 37 C.F.R. 1.75(d)(1)

In paragraph (2), the examiner objected to claims 29-30 as creating confusion since they were dependent from claim 31. Applicant has amended claims 29-30 to recite their dependency from claim 21. Applicant thanks the examiner for pointing out this discrepancy.

C. Claim Rejections under 35 U.S.C. § 101

In paragraphs (3-3.5) the Examiner rejected claims 3-6 and 13-49 under 35 U.S.C. 101 on the grounds that the invention is directed towards non-statutory subject matter.

C(1). Examiner's Grounds for Rejection of Claims 3-6 and 13-49 as nonstatutory under 35 U.S.C. § 101

The examiner stated the following in rejecting the claims as nonstatutory.

3.1 Claims 3-6 and 13-49 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The invention claims (claim 3 preamble), "*A method of determining aggressor-induced delay change in a victim net of stage of an integrated circuit design.*"

3.2 MPEP Section 2106(IV)(B)(2)(b)(ii) provides that a statutory computer process is determined not by how the computer performs the process, but by what the computer does to achieve a practical application with a useful, concrete and tangible result. For example, a computer process that simply calculates a mathematical algorithm

that models noise is nonstatutory, while a claimed process for digitally filtering noise employing the mathematical algorithm is statutory. The long line of cases in this area that are referred to in MPEP Section 2106(IV)(B)(2)(b)(ii) exemplify this requirement, by utilizing in the claim language, terms such as controlling, executing, changing and removing. In view of the aforementioned requirement and the interim guidelines for 101 eligibility, the Examiner respectfully contends that the claim language of independent claims 3, 13, 19, 21, 31, 34 and 40 do not claim a practical application with a tangible result, that language claiming: in claim 3:

providing (emphasis added) an input and output voltage;

producing a model of an interconnect network of the stage;

determining nominal delay in the stage;

providing a signal transition;

propagating a driver model output waveform;

determining noisy delay in the stage;

providing a signal transition;

providing at least one aggressor-induced voltage waveform;

propagating a driver model output waveform;

providing at least one aggressor-induced voltage waveform; and

determining a difference between the delays.

3.3 For at least these reasons, the Examiner respectfully posits that the claims of the present invention do not meet the criteria for a statutory process. Accordingly, the claims are determined to be a method of determining aggressor-induced delay change in a victim net of stage of an integrated circuit design, consisting solely of mathematical operations, converting one set of numbers into another set of numbers, whereby the method does not manipulate appropriate subject matter, and thus cannot constitute a statutory process (MPEP Section 2106(IV)(B)(2)(c)).

3.4 The Examiner also posits that the method of the present invention is computer executable software code, or a program per se, consisting of software instructions that implement the method of determining aggressor-induced delay change in a victim net of stage of an integrated circuit design. For at least this reason, the software instructions of the present invention do not manipulate appropriate subject matter, and thus cannot constitute a statutory process (MPEP Section 2106(IV)(B)(2)(c)).

3.5 In view of the aforementioned requirement, the Examiner respectfully contends that the claim language of independent claim 31 does not claim a practical application, that language claiming a computer readable medium encoded with a data structure representing a current model of a gate circuit. The medium holding a data structure is determined to recite data embodied on a computer-readable medium. However, the data does not impart functionality to either the data as claimed or to the computer. As such, the claimed invention recites nonfunctional descriptive material, *i.e.*, mere data. Non-functional descriptive material is merely carried on the medium, it is not structurally and functionally interrelated to the medium, and thereby does not manipulate, or execute, appropriate subject matter, and thus cannot constitute a statutory process (MPEP Section 2106(IV)(B)(2)(c))."

C(2). Applicant's Traversal of Rejection of Claims 3-6 and 40-49 under 35 U.S.C. § 101

Applicant respectfully traverses the examiner's Section 101 rejection of claims 3-6 and 40-49 as amended for the following reasons. Applicant respectfully submits that claims 3-6 and 40-49 as amended recite both a physical transformation and a practical application involving a method of determining aggressor-induced delay change in a victim net of a stage of an integrated circuit design.

C(2)(a). Claim 3 as amended recites a method recites a computer-implemented method

The preamble of claim 3 as amended recites a computer-implemented method and is not a mere series of mental steps.

C(2)(b). Claim 3 as amended recites a physical transformation

Applicant respectfully submits that claim 3 recites physical transformation of a signal that represents a real world phenomenon, and on that basis, recites statutory subject matter and not a mere abstract idea or mathematical operation.

In summary form, independent claim 3 as amended recites the steps of,

"providing...current model...;

producing a model of a load...;

producing a model of the interconnect network...;

simulating behavior of the victim net during nominal (noiseless) transition by performing steps including,

providing a signal transition at an input of to the driver gate;

using the current model of the driver gate and the load model of the interconnect network to produce a nominal driver gate output waveform resulting from the provided input signal transition;

using the interconnect model to propagate the nominal driver gate output waveform from the driver gate output to the receiver gate input;

simulating behavior of the victim net during noisy transition by performing steps including,

providing a signal transition at an input of the driver gate;

providing an aggressor-induced current waveform to an output of the driver gate;

using the current model of the driver gate and the load model of the interconnect network to produce a noisy driver gate output waveform resulting from the provided input signal transition and the aggressor-induced current waveform;

using the interconnect model to propagate the noisy driver gate output waveform from the driver gate output to the receiver gate input;

providing an aggressor-induced voltage waveform to an input of the receiver gate; and

producing a value representing a difference between delay associated with the simulated noiseless transition and delay associated with the simulated noisy transition." (Emphasis added)

Claim 3 recites a physical transformation of the driver model output waveform brought about by the "aggressor-induced current waveform". Specifically, claim 3 calls for, "providing at least one aggressor-induced current waveform." A driver model output waveform simulates a physical real world driver gate output signal. An "aggressor-induced current waveform simulates the result of a physical phenomenon referred to as cross-talk caused by capacitive coupling among nets in a circuit design. (See patent specification paragraphs [002]-[005].) Claim 3 calls for the interconnect network model *during nominal (noiseless) simulation*, "to propagate a nominal driver model output waveform" Claim 3 further calls for the interconnect network model *during noisy simulation*, "to propagate a noisy driver model output waveform, resulting from the provided signal transition and the aggressor-induced current waveform".

Therefore, the signals in claim 3 represent physical world signals: a the driver output waveform and an aggressor-induced current waveform. Claim 3 recites a transformation that represents a real physical world transformation. Specifically, the driver model output waveform (which represents a real world physical signal) is transformed by the aggressor-induced current waveform (which represents a physical real world signal).

Claim 3 recites a driver gate output waveform during the *noisy simulation* that is different from the driver gate output waveform during *nominal simulation* due to the aggressor-induced current. The aggressor-induced current waveform causes a physical transformation of the driver gate output waveform as between the *nominal* and *noisy* cases. The delay change "value" produced in the last step of claim 3, quantifies this physical transformation in terms of a difference in delay associated with the simulated *nominal* and the simulated *noisy* transitions. Therefore, claim 3 recites a statutory process since it recites a physical transformation of the driver output signal.

C(2)(c). Claim 3 as amended recites a practical application

Applicant respectfully submits that the method of claim 3 produces a useful, concrete and tangible result, and therefore, constitutes a practical application of the claimed method.

Applicant respectfully submits that in evaluating a claim to determine whether it produces a useful, tangible and concrete result, the focus is not on whether the *steps taken* to achieve a particular result are useful, tangible and concrete, but rather, whether the *result* itself is useful, tangible and concrete.

In the following sections, Applicant separately addresses the utility requirement, tangible result requirement and the concrete result requirement.

C(2)(c)(i). Claim 3 has utility

The invention of claim 3 has specific and substantial utility. There has been a need for an improved method to evaluate crosstalk effects on delay during the design of integrated circuits. The invention of claim 3 meets this need.

The need for evaluation of cross-talk delay during circuit design is explained in the BACKGROUND section at paragraph [0003],

"[0003] ...For example, crosstalk delay has become a more prominent element of timing analysis during integrated circuit design due to factors such as, (i) increase in coupling-to-total capacitance ratio, (ii) decrease in supply voltage resulting in a reduction of gate overdrive (iii) shortening of clock period causing transition waveforms to play a bigger role, and (iv) tighter timing margins requiring more accurate timing analysis and less overestimation of delay."

Cross-talk delay can cause distortion as explained in the BACKGROUND section at paragraph [0006],

"[0006] Another challenge with analyzing a crosstalk induced delay change arises from the potential for crosstalk to distort a victim switching waveform. A distorted waveform may deviate from the input waveforms used in delay characterization of a receiving gate, resulting in inaccuracy in slew dependent delays in a downstream logic cone. If the crosstalk impact is severe, the victim waveform may even become non-monotonic (bumpy), the effect of which may not be properly modeled in existing gate delay systems."

The distortion resulting from cross-talk can make it even more difficult to evaluate cross-talk delay. As explained in the BACKGROUND section in paragraphs [0010]-[0011],

Figures 14A-14B illustrate signal distortion problems associated with aggressor waveforms.

"[0010] ...Figure 14A is an illustrative drawing of a set of curves that represent victim signal transitions from V_{DD} to ground. Each curve represents a different alignment of a victim signal transition with an aggressor signal. In each case, the aggressor signal induces a bump in the victim signal transition. The curves are non-monotonic due to the aggressor-induced bumps. Victim net signal transition delay is measured in terms of the time at which the victim signal crosses the V_{ref} level. The curves of Figure 14A illustrate that an aggressor-induced bump can cause the victim signal to cross V_{ref} multiple times. A second crossing increases the measured victim signal transition delay according to the conventional methodology, since the delay should be measured based on the latest crossing of V_{ref} .

[0011] Figure 14B is an illustrative drawing of a curve representing victim signal transition delay versus aggressor alignment. The heavy dots on the delay curve denote correspondent crossing times of V_{ref} on the noisy transitions shown in Figure 14A. The curve of Figure 14B shows that victim signal transition delay depends upon aggressor alignment. Unfortunately, the non-monotonic waveforms of Figure 14A result in a 'cliff' in the curve of Figure 14B methodology. The last curve in Figure 14A does not have a bump crossing V_{ref} , which engenders the cliff in delay curve in Figure 14B. This prior methodology is not robust because even a relatively small change in a circuit parameter (e.g., driver size, supply voltage, etc) and/or aggressor alignment on a particular victim net can result in a disproportionate change in measured victim signal delay due to the such cliff."

The DETAILED DESCRIPTION at paragraphs [0036]-[0037] describes "aggressors" and their impact upon delay change in a "victim net".

"[0036] A victim net is a net for which crosstalk delay change is to be analyzed. An aggressor net is a net coupled through parasitic capacitance to the victim net. A stage is a victim net, its aggressor nets and their driving gates. It will be appreciated that a given net may be characterized as a victim net at one point in a timing

analysis and may be characterized as an aggressor net at other points in the timing analysis.

[0037] Crosstalk delay change is a difference between crosstalk delay and nominal delay. Crosstalk (stage) delay change is the extra delay in a victim net state change (switching from logic 0 to 1 or from logic 1 to 0) induced by transitioning of some or all aggressors of the victim net. In general, for crosstalk delay analysis, the maximum of crosstalk delay change (taken absolute value) is of greatest interest. The delay change is positive when victim and aggressors switch in opposite directions and it is used for *late* arrival time calculation (often referred to as *max delay analysis*). Similarly, the delay change is negative when victim and aggressors switch in opposite directions and it is used for *early* arrival time calculation (often referred to as *min delay analysis*). Nominal (stage) delay is a stage delay when aggressors are held quiet (logical 0 or 1)."

The DETAILED DESCRIPTION section at paragraph [0038] explains that at least some prior methods of determining aggressor-induced delay change often were overly pessimistic, signifying a need for an improved method of determining aggressor-induced delay change.

"[0038] **Figure 1** shows an example of the type of problem associated with aggressor alignment and delay measurement based on a predefined waveform crossing threshold. Waveform 102 is provided on a victim receiver input. Waveform 104 is provided on a victim receiver output. Waveforms 102 and 104 are noisy (i.e., impacted by aggressors). The receiver gate in this example is an inverter. The waveforms in the example are computed in Spice using an exhaustive sweep of alignment parameters on a victim net in a 0.13 micron industrial design. The worst-case delay pushout when measured at the 50% Vdd crossing is 724ps (Typically, V_{ref} is chosen as 50% Vdd, but sometimes, especially when skewed gates dominate, it is less than that). This can happen when a rising receiver input waveform 102 has a falling noise bump 106 that barely touches the threshold and then rises again. However, this bump on the receiver input waveform 102 causes almost no delay change in the receiver output waveform 104 where the transition has only a slight bump 108 at the end. The receiver, a CMOS gate, in essence acts as a low pass filter, thereby smoothing the signal. Thus,

aggressor alignment based on a conventional delay metric (50% V_{dd} crossing) applied to the bumpy transition on the victim net is clearly too pessimistic. Measurement of transition time using a V_{ref} crossing time of the non-monotonic waveform is non-robust and can lead to non-unique results."

The DETAILED DESCRIPTION section provides an overall explanation of the delay change calculation at paragraph [0083].

"[0083] An overall delay change calculation process in accordance with one embodiment for determining victim net signal delay change caused by aggressor induced crosstalk will be discussed next. By way of overview, pre-computed aggressor waveforms are used to determine aggressor induced current in a victim net. The aggressor-induced current, together with a current model (CM) of a (selected) victim net driver with a Π -load which is determined from a perspective of the driver output, is used to determine the driver output voltage V_{out} of the selected victim net driver. A computational model of interconnect involving a transfer function $H(s)$, determined for an interconnect network comprising the victim net and its aggressor nets, is used to propagate a determined victim driver output voltage V_{out} signal to a (selected) receiver input. The pre-computed aggressor waveforms are used to determine aggressor induced current and voltage responses at, respectively, driver output and the receiver inputs using the computational model of the interconnect involving the functions $H(s)$, $Y(s)$, as shown in Figure 16. An overall receiver input voltage waveform is determined based upon the aggressor induced victim receiver input voltage plus the voltage waveform propagated to the receiver input based upon the driver output voltage waveform. A current model of the (selected) receiver is used to propagate an overall receiver input voltage signal to the receiver output based upon the overall voltage at the receiver input. Crosstalk delay change is determined based upon two waveforms (noisy and noiseless) calculated at the receiver output." (Emphasis Added)

The DETAILED DESCRIPTION section points out in paragraph [0089] that in the disclosed embodiment, crosstalk delay change is defined in terms of a difference in transition times on *noisy* and *nominal* transitions of a stage's output caused by the same transition on the stage's input.

"[0089] The maxrise crosstalk delay change on the j-th stage's output is defined as the difference in transition times as measured using some transition time functional J on noisy and nominal transitions on the stage's output caused by the same (late or early) transition on one of the stage's inputs:

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Therefore, the invention of claim 3 has specific and substantial utility. The invention of claim 3 meets a specific need in a substantial way, for an improved method to evaluate aggressor-induced crosstalk delay during the design of integrated circuits.

C(2)(c)(ii). Claim 3 produces a tangible result

The invention of claim 3 produces a tangible result - a value representing a difference between delay associated with the simulated noiseless transition and delay associated with the simulated noisy transition. As explained in paragraphs, [0086]-[0090], for example, such aggressor-induced delay change is used to more accurately simulate the propagation of a signal through an integrated circuit design during static timing analysis (STA).

"[0086] The following discussion defines the crosstalk delay change for an example situation in which there is a *maxrise* transition on a victim net denoting late rising transition. The three other types of transitions (*maxfall*, *minrise* and *minfall*) that are propagated through a design during static timing analysis (STA) can be defined similarly. Maxrise and minrise transitions on a victim denote transitions in which the output of the victim driver transitions from 20% of Vdd to 80% of Vdd are latest and earliest possible, respectively. Maxfall and minfall transitions on a victim driver denote transitions in which the output of the victim driver from 80% Vdd to 20% Vdd is latest and earliest possible, respectively.

[0087] First, let $J[V(t)]$ denote a function over a space of rising or falling transitions. The value J is used as a transition time metric which associates a number (transition time) to a transition waveform. The conventional transition time metric, denoted by J_{ref} , is defined as the time when transition crosses V_{ref} (typically 50% Vdd).

[0088] The maxrise nominal output transition, $\overline{X}_j(t)$ is defined as a rising transition occurring on j-th output of the stage (on an input of j-th receiver) caused by a late transition on one of the stage's inputs and with all aggressors being "quiet". Similarly, the maxrise noisy transition, $\tilde{X}_j(t)$ is defined as a rising transition with the aggressors undergoing falling transitions.

[0089] The maxrise crosstalk delay change on the j-th stage's output is defined as the difference in transition times as measured using some transition time functional J on noisy and nominal transitions on the stage's output caused by the same (late or early) transition on one of the stage's inputs:

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[0090] Transitions on the victim and aggressor nets can occur within corresponding switching windows (separately for rising and falling transitions) calculated during STA and specified relative to some (possibly different) clocks. Let W_k , $k = 0, \dots, N$ denote switching windows (SW) on the victim and aggressor nets. It is assumed in this example that the SW's of the aggressor nets belong to the same clock domain as SW for the victim net. If clocks of an aggressor and the victim net are asynchronous, the aggressor's switching windows can be set to be infinitely wide. In this example, it is assumed that a SW is a range $W_k = [\tau_{ek}, \tau_{lk}]$, with the boundaries τ_{ek} , τ_{lk} being, respectively, the earliest and latest possible transition times as determined during STA on k-th aggressor."

Thus, the method of claim 3 produces a delay change value, which is a tangible result representing the difference in delays associated with simulated *nominal* and *noisy* transitions. This delay change value can be tangibly used during static timing analysis (STA) to more accurately represent the impact of cross-talk delay upon circuit behavior. STA results, in turn, are used in developing and refining an integrated circuit design.

C(2)(c)(iii). Claim 3 produces a concrete result

The invention of claim 3 produces a concrete result. The delay change value is repeatable. In fact, an aspect of one embodiment of the invention involves a constrained

optimization-based search for WC (worst case) aggressor alignment for determining delay changes for different aggressor alignments in order to identify a worst case aggressor alignment. Such WC searching requires accurate repeatability to achieve convergence on a WC aggressor alignment. (See patent specification at paragraphs [0117]-[0139].

C(2)(c)(iv). Claims 4-6 and 40-49 constitutes statutory subject matter for the same reasons as for claim 3

Claim 3 is an independent claim from which claims 4-6 depend. Therefore, claims 4-6 constitute statutory subject matter for the same reasons set forth above for claim 3.

Moreover, Applicant respectfully submits that the arguments set forth for above for claim 3 are applicable, in general, to claims 40-49, and for that reason, claims 40-49 also constitute statutory subject matter.

C(3). Applicant's Traversal of Rejection of Claims 13-30 under 35 U.S.C. § 101

C(3)(a). Independent claim 13 as amended recites an article of manufacture encoded with an information structure representing a gate circuit

Claim 13 as amended recites,

"13. An article of manufacture including a computer readable medium encoded with an information structure representing a driver circuit, the information structure comprising:

a current model that associates instantaneous values of input node voltage, output node voltage and output node current of the driver circuit;

a model of capacitance between an input node and an output node of the driver circuit; and

a model of capacitance between the output node of the driver circuit and a ground potential."

The recited information structure has functional interrelationships with computer software and hardware that permit the data structure's functionality to be realized. For example, as explained in the specification at paragraph [0079], in one embodiment, the current model comprises a ViVo model that serves as a nonlinear current model.

"[0079] The ViVo model of **Figure 6A** is employed as the nonlinear current model 626 in the embodiment of **Figure 6A**. ViVo models current response of the last CCC, such as component 608 of **Figure 6A**, of a driver 606 to voltages on input and output. The ViVo model is pre-characterized and stored in a cell library per each transition type (rise/fall) and per each input-output arc of each interface CCC of the cell, that is a CCC connected to either input or output pin of the cell CCC. ViVo models current drawn by the output pin of the CCC for various voltage values on the input and output pins. This current model is part of an embodiment of the invention that allows high accuracy of analysis due to the fact that a current drawn by a gate during switching can be well represented by a voltage-controlled current source, which is a function of instantaneous voltages on the input and output: $I_d = I(V_i, V_o)$. It is implemented as a two dimensional (2-D) current table, discussed below, describing the nonlinear (voltage-controlled) current source. In addition to the 2-D current table shown in **Figure 6B**, the ViVo CM also includes two capacitors modeling, respectively, the Miller C_M and ground C_g capacitance of the output pin of the output of the CCC, shown in **Figure 6A**."

As explained in paragraphs [0081]-[0082], the current model is used to determine the impact of aggressor-induced current upon victim driver output node voltage.

"[0081] A vertical axis of the 2-D table lists V_{in} values V_{i0} to V_{iM} . A horizontal axis of the 2-D table lists V_{out} values V_{o0} to V_{oN} . Entries in the table are current values associated with voltage value pairs (V_{in}, V_{out}) . For instance, current value I_{22} is associated with the pair (V_{i2}, V_{o2}) , and I_{M2} is associated with the pair (V_{iM}, V_{o2}) . Conversely, a V_{out} value is associated with a $(V_{in}, \text{current value})$ pair. For example, $V_{out}=V_{o2}$ is associated with the pair, (V_{iM}, I_{M2}) .

[0082] Therefore, the ViVo model advantageously can be used to assess the impact of aggressor induced victim current upon driver output node voltage V_{out} in a victim net. More particularly, the value of an output voltage V_{out} of a ViVo model of a CCC depends upon a combination of a value of an input voltage V_{in} provided to the ViVo model and a value of current drawn through the ViVo model. As explained more fully below, pre-computed aggressor waveforms are used during crosstalk analysis to produce a

composite aggressor induced current in the victim net. The composite aggressor induced current is the sum of aggressor induced currents from all aggressor nets. In the simplified drawing of **Figure 6A**, only one aggressor net 604 is shown. However, a given victim net in a real IC design may have multiple aggressor nets, each capable of inducing a current on the victim net. Aggressor induced current in a victim net contributes to the current drawn by the ViVo model. Specifically, the aggressor induced current in a victim net contributes to the current drawn by the driver (model) defined by the table as $I(V_{in}, V_{out})$ and the current drawn by the load represented by the PI-load model. The Kirchhoff current law (KCL) is then used to determine output voltage V_{out} of the ViVo model in an iterative numerical procedure. Thus, as explained more fully below, a current model of a victim net driver can be used to calculate a voltage transition on the driver (model) output and therefore to assess delay change due to crosstalk."

Figures 13A-13C illustrate the overall flow of a computer program implemented process to determine aggressor-induced delay change. Paragraphs [0142] and [0146] describe the functional interrelationship between a victim net driver current model and the computer program implemented process. Paragraphs [0143] and [0147] describe the functional interrelationship between a victim net receiver current model and the computer program implemented process.

Therefore, claim 13 as amended recites an article of manufacture encoded with a,

"a current model that associates instantaneous values of input node voltage, output node voltage and output node current of the driver circuit;"

The association provided by the current model, between instantaneous values of input node voltage, output node voltage and output node current has a functional relationship with the computer program code of **Figures 13A-13C** that permit the current model's functionality to be realized.

C(3)(b). Claims 14-30 constitutes statutory subject matter for the same reasons as for claim 13

Claim 13 is an independent claim from which claims 14-20 depend. Therefore, claims 14-20 constitute statutory subject matter for the same reasons set forth above for claim 13.

Furthermore, Applicant respectfully submits that the arguments set forth for above for claim 13 are applicable, in general, to claims 21-30, and for that reason, claims 21-30 also constitute statutory subject matter.

C(4). Applicant's Traversal of Rejection of Claims 31-33 under 35 U.S.C. § 101

C(4)(a). Independent claim 31 recites an article of manufacture encoded with an information structure produced according to a process defined in the claim

Claim 31 recites the following,

"31. An article of manufacture including a computer readable medium encoded with a current model of a driver circuit, the current model associating input voltage values, output voltage values and current values, the current model produced by a process including the steps of:

for each of a plurality of different pairs of first and second DC voltage values,

sensitizing an input node of a cell model representing the driver circuit with a first DC voltage value; and

sensitizing an output node of the cell model with a second DC voltage value; and

generating a value of current drawn by the output node of the cell model based upon the provided first DC voltage value and the provided second DC voltage value."

As will be appreciated from the specification at paragraph [0080], the steps of the method set forth in claim 31 are performed by a computer program process. In one embodiment, the method involves a series of DC simulations using the Spice simulation program.

"[0080] Since the ViVo current table is a function of instantaneous voltages on input and output and not dependent on transition history, its generation can be done through a series of DC simulations in Spice and can be very fast. The capacitances C_M and C_g are obtained in one embodiment as a sum of parasitic capacitances of devices

in the gate. In another embodiment they can be computed using transient simulation in Spice. In a present embodiment, sensitization for DC simulations is determined from a logic function extracted from the CCC using binary-decision diagrams (BDD). Each DC simulation is performed for a pair of constant voltages on input/output pins, and generates an entry in the 2-D current table. In a present implementation, as a part of the characterization carried out for multi-CCC cells additional to the ViVo CM, the slew is characterized for the last CCC's inputs as a function of slews on the cell's inputs."

Moreover, it will be appreciated that the current model of a driver circuit recited in the preamble of claim 31 is akin to the current model of claim 13. Therefore, as explained with reference to claim 13, the current model recited in the claim 31 preamble has a functional interrelationship with computer software and hardware that permit its functionality to be realized.

Therefore, applicant respectfully submits that claim 31 constitutes statutory subject matter.

C(4)(b). Claims 32-33 constitute statutory subject matter for the same reasons as for claim 31

Claim 31 is an independent claim from which claims 32-33 depend. Therefore, claims 32-33 constitute statutory subject matter for the same reasons set forth above for claim 31.

C(5). Applicant's Traversal of Rejection of Claims 34-39 under 35 U.S.C. § 101

C(5)(a). Independent claim 34 recites an article of manufacture encoded with an information structure produced according to a process defined in the claim

Claim 34 recites the following,

"34. An article of manufacture including a computer readable medium encoded with instructions for performing a method of simulating aggressor-induced behavior of a driver circuit and an interconnect network driven by the driver circuit, the method comprising:

providing a voltage signal transition on an input of a current model representing the driver circuit, the current

model associating instantaneous values of input voltage, output voltage and output current of the driver circuit;

providing an aggressor induced current waveform on a node interconnecting an output of the current model and a load model representing the interconnect network, the load model approximating output point admittance of the interconnect network; and

using the current model and the load model to produce a voltage waveform on the output of the current model based upon the received input voltage signal transition and the received aggressor induced waveform."

Applicant respectfully submits that claim 34 as amended constitutes statutory subject matter.

C(5)(b). Claims 35-39 constitute statutory subject matter for the same reasons as for claim 34

Claim 34 is an independent claim from which claims 35-39 depend. Therefore, claims 35-39 constitute statutory subject matter for the same reasons that claim 34 does.

D. Examiner's Grounds for Rejection of Claims 13, 19, 21-23, 27, and 31-33 as anticipated under U.S.C. § 102(b)

The examiner stated the following in rejecting the claims as anticipated.

"4.1 Claims 13, 19, 21-23, 27, and 31-33, are rejected under U.S.C. 102(b) as being anticipated by the article authored by Keller et al., entitled *A Robust Cell-Level Crosstalk Delay Change Analysis*.

4.2 The article by Keller et al., cited on the 1449 received on 19-July-2004, but not citing a publication date, discloses: in section 3.1, entitled *Vivo: precharacterized gate current model*, and Figure 5, each of the limitations of claims 13, 19, 21-23, 27 and 31-33, including: a current model associating instantaneous input and output voltages and a current source; models of capacitance between input and output nodes, and an output node and a ground potential; a model of Miller capacitance; and sensitization for DC simulations, including a 2-D current table and constant DC voltage values."

D(1). Applicant's Traversal of Rejection of Claims 13, 19, 21-23, 27, and 31-33 under U.S.C. § 102(b)

Applicant respectfully traverses the rejection of claims 13, 19, 21-23, 27, and 31-33 under U.S.C. § 102(b) for the following reason. Neither of the two documents identified in the Form PTO-1449 received on 19-July-2004 and used by the examiner as the basis for the rejection constitutes a prior art printed publication. As noted by the Examiner, the Form PTO-1449 does not list a publication date for either of these documents. The reason that no publication date is indicated is that as of the filing date of the instant patent application (December 12, 2003), neither of the two referenced documents had been published.

By way of further explanation, the two documents referenced by the examiner and listed on the PTO-1449 are earlier drafts of a technical paper that was used as a starting point for the instant patent application. Apparently, due to a clerical oversight, these two documents were listed in the PTO-1449 despite the fact that neither of them had been published as of the date of the filing of the instant patent application.

Enclosed for the Examiner's information is a Supplemental PTO-1449 listing a technical paper (copy enclosed) that eventually was published in, Igor Keller, Ken Tseng and Nishath Verghese, "A robust cell-level crosstalk change delay analysis", *IEEE, ICCAD 2004*, presented November 8, 2004, which not constitute prior art to the instant invention.

E. Examiner's Claim Objections

The Examiner indicated that,

"5. Claims 14-18, 20, 24-26, and 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims."

F. Examiner's Indication of Allowable Claims

The Examiner indicated that,

"6. Claims 3-6 and 34-39 are deemed allowable over the prior art of record at this time, pending resolution of the rejections noted above."

IV. Amendments to the Claims

Applicant has amended claims 3, 5, 6, 13-31, 34-40 and 48-49. Applicant has added new claims 50-66.

Claim 3

The preamble of claim 3 has been amended to make explicit the constituents of the recited "stage". These constituents had been implicit in claim 3 prior to such amendments. Certain additional amendments also have been made to claim 3 to explicitly relate elements of claim 3 with elements of the "stage" recited in the preamble as amended.

Amendment of Claims 3 and 40

Claims 3 and 40 have been amended to recite,

"...simulating behavior of the victim net during nominal (noiseless) transition by performing steps including,...

simulating behavior of the victim net during noisy transition by performing steps including,...

producing a value representing a difference between delay associated with the simulated noiseless transition and delay associated with the simulated noisy transition."

Claims 3 and 40 were amended to include the above language. These amendments were not made for a purpose related to patentability but rather to make explicit in these claims what had been implicit in these claims. That is, that simulations of nominal (noiseless) and noisy transitions are performed, and that a value is produced representing a difference in delays associated with the simulated nominal and noisy transitions.

Claim 3 also has been amended to recite,

"...producing a model of a load presented to an output of the driver gate by the interconnect network;...

using the current model of the driver gate and the load model of the interconnect network to produce a nominal driver gate output waveform resulting from the provided input signal transition;...

using the current model of the driver gate and the load model of the interconnect network to produce a noisy driver gate output waveform resulting from the provided input signal transition and the aggressor-induced current waveform;...”

Claim 3 was amended to include the above “producing” and “using” language in order to make explicit in claim 3 what had been implicit in the claim. Specifically, claim 3 as amended makes clear that current model of the driver gate and the load model of the interconnect network are used to produce both the nominal and noisy driver gate output waveforms, and that the load model represents the load presented to the driver output by the interconnect network.

Similar amendments are made to claim 40 with respect to, “using the driver circuit current model and the load model”. A reason for these amendments to claim 40 is to make explicit in claim 40 what had been implicit in the claim.

Claims 13-30 and 34-39

Claims 13-30 and 34-39 have been amended to recite article of manufacture in order to meet the statutory subject matter requirement.

New Claims 50-54

New claims 50-54 depend from currently amended independent claim 3.

New Claims 55-56

New claims 55-56 depend from currently amended independent claim 40.

New Claim 57-60

New article of manufacture claim 57 generally corresponds to currently amended claim method claim 3. New claims 58-60 depend from new claim 57.

New claims 61-66

New claim article of manufacture claim 61 generally corresponds to method currently amended claim 40. New claims 62-66 all (ultimately) depend from new claim 61.

Claims 6, 50, 55, 56, 59, 60, 61, 62 and 63 relate to “receiver” output waveforms

Note that dependent claims 6, 50, 55, 56, 59, 60, 61, 62 and 63 set forth limitations relating to producing "receiver" output waveforms.

Claim 6

Claim 6 has been amended to conform its language to that of claim 3 as amended. Examples of support for nominal and noisy propagation through a receiver model are provided in paragraphs [0143] and [0147].

Driver circuit replaces gate circuit for consistency

The term "driver circuit" has been inserted in place of the term "gate circuit" in many of the claims for consistency. This amendment does not and is not intended to narrow the claims.

Removal of unnecessary "data structure" limitations

Unnecessary language referring to "data structure" has been omitted from claim 31.

Other Amendments

Various other amendments have been made to the claims for the purpose of making explicit what had been implicit.

No New Matter

Applicant respectfully submits that no new matter has been added through any of the above these amendments.

V. Supplemental Information Statement

Applicant has submitted herewith Supplemental Information Disclosure Statement identifying the following reference (which is not prior art),

Igor Keller, Ken Tseng and Nishath Verghese, "A robust cell-level crosstalk change delay analysis", *IEEE, ICCAD 2004*, presented November 8, 2004.

CONCLUSION

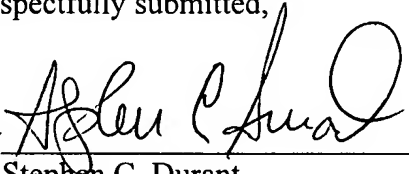
Applicant respectfully submits that the claims as amended are allowable. Applicant respectfully requests reconsideration, passage to issuance and allowance of the claims as amended.

* * * * *

In the unlikely event that the transmittal form is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing **Docket No. 188122000400**. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: January 23, 2007

Respectfully submitted,

By 

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